The Phase-II ATLAS Pixel Tracker Upgrade: Layout and Modules

ATLAS II fazes pikselinio trakerio modernizavimas: išdėstymas ir moduliai

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In the high-luminosity era of the Large Hadron Collider (the HL-LHC), the instantaneous luminosity is expected to reach unprecedented values, resulting in about 200 proton-proton interactions in a typical bunch crossing. To cope with the resulting increase in occupancy, bandwidth and radiation damage, the ATLAS Inner Detector will be replaced by an all-silicon system, the Inner Tracker (ITk). The innermost part of ITk will consist of a state-of-the-art pixel detector, with an active area of about 14 $m^{2,}$ which will provide tracking capability up to $|\eta| = 4$. The pixel system will consist of approximately 10,000 pixel modules and over $5x10^9$ pixel detector elements. The layout of the ITk pixel system will be described based on the ATLAS ITk pixel Technical design proposal [1].

In order to cope with the changing requirements in terms of radiation hardness, power dissipation and production yield, several different silicon sensor technologies will be employed in the five barrel and endcap layers. The innermost layer will feature 3D silicon sensors, due to their inherent radiation hardness and low power consumption, while the remaining layers will employ planar silicon sensors with thickness ranging from 100 µm to 150 µm. All hybrid detector modules will be read out by novel ASICs, implemented in 65 nm CMOS technology and thinned to 150 µm, which will be connected to the silicon sensors using bump bonding.

With the arrival of the first readout chip prototype, the RD53A chip, prototype modules are being built to study sensor and chip properties, thermal performance, as well as bump bonding yield in lab measurements and beam test campaigns. Irradiation studies are ongoing to validate the design for the full operational lifetime of the ATLAS ITk.

In addition, the development of hybrid detector modules is starting to address numerous production issues, understanding of which will be crucial for the layout and production of the final ITk pixel detector modules. Due to the size of the pixel system and the power constraints for the first time in a particle physics experiment the modules will be connected in a serial powering chain, which gives further challenges. A large prototyping programme on system test level is ongoing. Components for larger structures with multiple modules based on the FE-I4 front-end chips were produced and are in assembly and evaluation. The paper will present latest results from the assembly and characterization of prototype modules as well as the latest evaluation and results of thermo-mechanical prototypes and fully electrical prototypes.

Two types of pixel sensors are developed to balance the required radiation tolerance, varying across the detector volume, with the production costs. The planar-type sensor (sketched in Fig. 1(a)) comes from a rather standard production process. The n+in-p structure has been chosen since it was shown to be more robust against type inversion than the p+-in-n type. The second type is the 3D-sensor, where n-type and p-type pillars runs vertically across the sensor (see Fig. 1(b)). The radiation tolerance of this structure is better than that of planar sensors because of the shorter collection distances. However, the production process is technically much more complex and expensive than in the case of planar sensors.

FE chips for the high rate collisions at the HL-LHC are required to achieve rapid readout with few GHz. The RD53 collaboration is developing a new type of FE chip for the ATLAS and CMS experiments at the HL-LHC [2] based on 65 nm CMOS technology. The target performance is a low noise rate with low threshold (<10−6 at a threshold of 600e−) with a data transfer rate of 1.28 Gbps. The latest chip, called RD53A, has been designed in such a way to allow the comparison of three different implementations of the analogue frontend which will be described. The sharp process line is expected to suppress the high rate of Single Event Upset (SEU), which is caused by a bit flip by injected particles into FE-chips. The evaluation of the efficiency and general features is ongoing by testbeam and irradiation and the latest results are reported here.

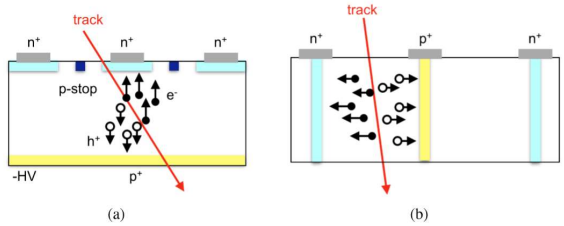

Fig. 1. Description of planar type sensor (a) and 3D type sensor (b)

Keywords: silicon pixel detectors, ATLAS, HL-LHC.

Literature

[1] ATLAS Collaboration, Technical Design Report for the ATLAS Inner Tracker Pixel Detector, CERN-LHCC-2017-021.
[2] RD-53 Collaboration, http://rd53.web.cern.ch/rd53/.